AmPAL*18P8

20-Pin IMOX™ Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- Individually programmable output polarity on each output
- Pin compatible superset of most combinatorial 20-pin PALs
- Eight logical product terms per output for increased logic power
- Increased input/output flexibility
  - 18 possible array inputs
  - Eight bidirectional I/Os with individually controllable output enable
- Ultra high-speed version t_{PD} = 15 ns maximum
- Superior quality
  - Full AC and DC parametric testing performed on every part
  - Extensive on-chip test circuitry ensures post-programming functional yield (PPFY) of 99.9%
- Platinum-Silicide fuses ensure high programming yield > 98%, fast programming and unsurpassed reliability

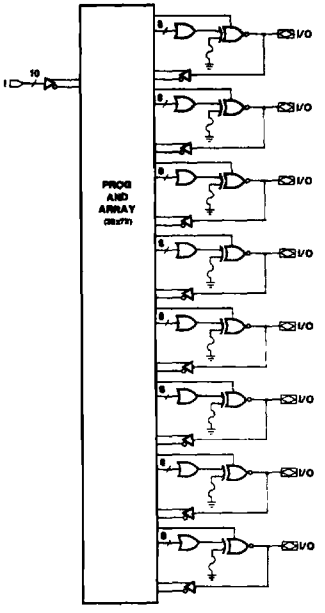
GENERAL DESCRIPTION

The AmPAL18P8 is an ultra high-performance, functionally enhanced 20-pin Programmable Array Logic element. It utilizes the familiar sum-of-products (AND-OR) structure allowing users to program custom logic functions to precisely fit their application.

The AmPAL18P8 offers significantly enhanced functional capabilities when compared to other combinatorial 20-pin PAL devices. These include two additional bidirectional I/O pins as well as additional product terms (bringing each output to eight logical and one three-state control product term) for extra logic power. The device also features individually user programmable output polarity, giving the designer the capability to handle both active HIGH and active LOW outputs on the same device.

A wide variety of speed/power selections is available, allowing precise matching to system requirements. The ultra high-speed version offers 15 ns maximum input to output propagation delay, opening up many new applications for the use of programmable logic.

BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

Family Part No.	AmPAL18P8									
Power Grade	Quarter Power		Half Power				Full Power			
Ordering Part No.	18P8Q		18P8L		18P8AL		18P8A		18P8B	
Speed Grade	Standard Speed				High Speed				Ultra High Speed	
Max. Access Time (ns)	STD	APL	STD	APL	STD	APL	STD	APL	STD	APL
	35	40	35	40	25	30	25	30	15	20
Max. Operating Current (mA)	55		90				180			

STD = AMD "Standard" products
APL = AMD "Approved Products List" products

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IMOX is a trademark of Advanced Micro Devices, Inc.

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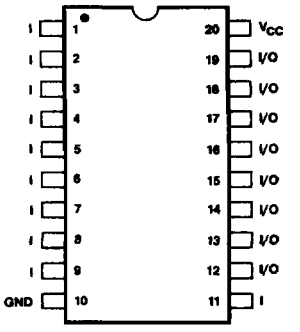
Issue Date: October 1986

CONNECTION DIAGRAMS
Top View



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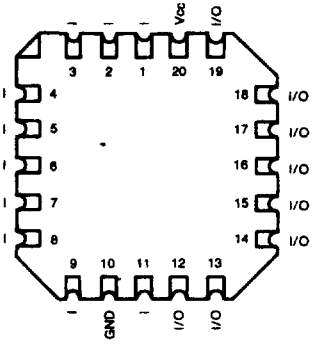
Note: Pin 1 is marked for orientation.

LCC*



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*Same Pinouts apply for PLCC.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed/Power Option
C. Package Type
D. Temperature Range
E. Optional Processing

AMPAL18P8 B P C —

E. OPTIONAL PROCESSING
Blank = Standard processing

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

C. PACKAGE TYPE
P = 20-Pin Plastic DIP (PD 020)
D = 20-Pin Ceramic DIP (CD 020)
J = 20-Pin Plastic Leaded Chip Carrier (PL 020)
L = 20-Pin Ceramic Leadless Chip Carrier (CL 020)

B. SPEED/POWER OPTION
B = Ultra High Speed/Standard Power
A = High Speed/Standard Power
AL = High Speed/Half Power
L = Standard Speed/Half Power
Q = Standard Speed/Quarter Power

A. DEVICE NUMBER/DESCRIPTION
AmPAL18P8
20-Pin IMOX Programmable Array Logic

Valid Combinations	
AMPAL18P8B	PC, DC, DE, JC, LC, LE
AMPAL18P8A	
AMPAL18P8AL	
AMPAL18P8L	
AMPAL18P8Q	

Valid Combinations

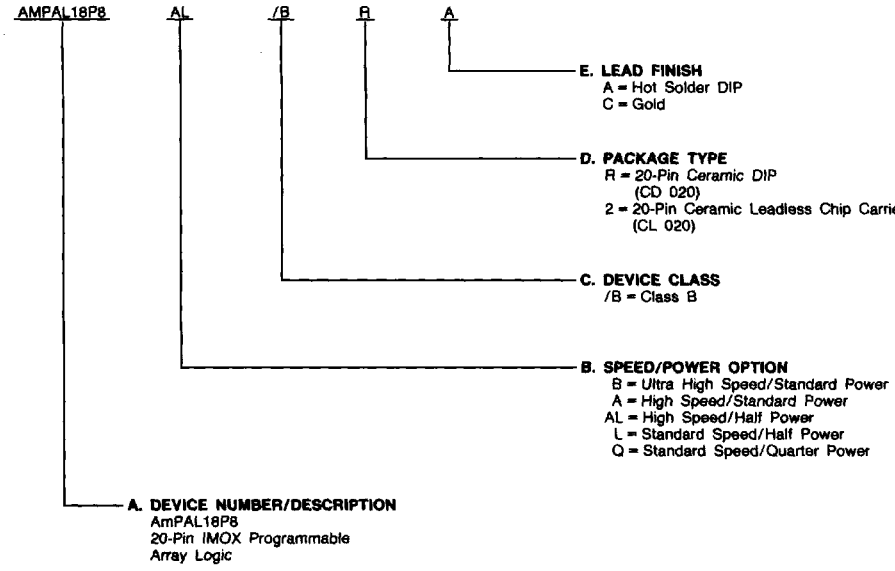
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

A. Device Number
B. Speed/Power Option
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AMPAL18P8B	/BRA, /B2C
AMPAL18P8A	
AMPAL18P8AL	
AMPAL18P8L	
AMPAL18P8Q	

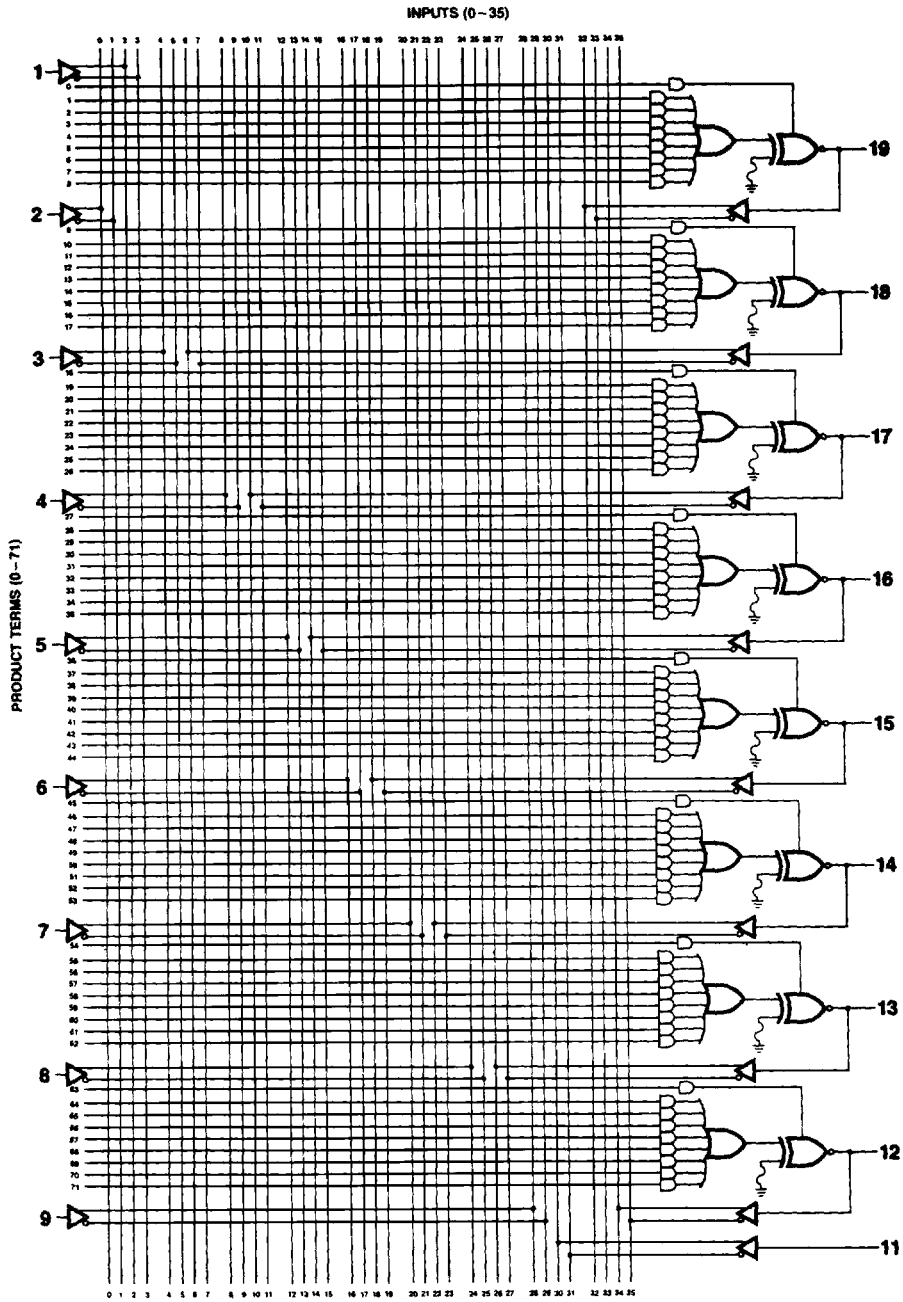
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11

LOGIC DIAGRAM



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Eighteen Array Inputs
- 10 dedicated
- 8 bidirectional I/O

Eight 8-Wide AND-OR Structures
- Combinatorial outputs
- Programmable output enable for each output
- Programmable polarity on each output

FUNCTIONAL DESCRIPTION

The AmPAL18P8 is a functionally enhanced Programmable Array Logic (PAL) device. The Block Diagram on page one shows the basic architecture of the AmPAL18P8. There are up to eighteen inputs and eight outputs available. The inputs are connected to a programmable AND array which contains 72 logical product terms. Initially the AND gates are connected, via fuses, to both the true and complement of every input. By selective programming of fuses, the AND gates may be "connected" to only the true input (by blowing the complement fuse) to only the complement input (by blowing the true fuse), or to neither type of input (by blowing both fuses), establishing a logical "don't care." When both the true and complement fuses are left intact, a logical false results on the output of the AND gate. An AND gate with all fuses blown will assume the logical true state.

The AmPAL18P8 has a possible maximum of 18 input pins, two more than previous 20-pin PALs. The extra inputs extend the functional capabilities of the device, which reduces design limitations, making it easier to design with and more flexible.

The AmPAL18P8 can be programmed with more complex logic equations due to the eight product terms and one control term for each output. The control terms also allow for each of the eight bi-directional I/Os to be three-stated, greatly expanding the realm of design possibilities.

The eight bi-directional I/O pins enhance the usefulness of the AmPAL18P8 by allowing for greater complexity of logic equations and hence more logic power.

The AmPAL18P8 also has programmable output polarity, giving the designer the choice of either active HIGH or active LOW on each of the eight outputs. This simplifies the task of programming the AmPAL18P8 and allows more freedom in optimizing the logic functions. The high-speed version of the AmPAL18P8 boasts 15 ns maximum input-to-output propagation delay, which makes it the fastest TTL-compatible PAL on the market today, and creates new possibilities for the use of programmable logic devices in a wide variety of applications.

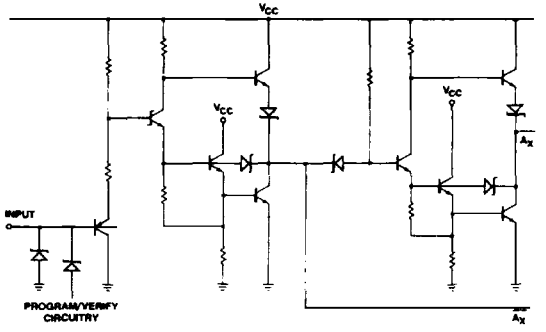
The AmPAL18P8 is manufactured using Advanced Micro Devices' IMOX oxide isolation process. This advanced process permits an increase in density and a decrease in internal capacitance, resulting in the fastest possible programmable logic devices. The AmPAL18P8 is fabricated with AMD's fast-programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Platinum-Silicide was selected as the fuse-link material to achieve a well-controlled melt rate, resulting in large non-conductive gaps that ensure very stable, long-term reliability. Extensive operating testing has proven that this low-field, large gap technology offers the best reliability for fusible link programmable logic.

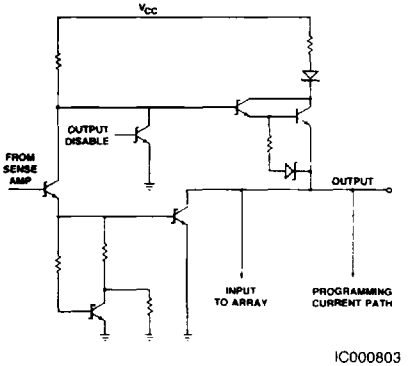
The AmPAL18P8 has been designed with extensive internal test circuitry that allows the programming and operating circuitry in the part to be thoroughly tested at the factory before programming. This assures excellent programming yield and functional performance to data sheet parameters after programming. The Post-Programming Functional Yield (PPFY) for this device is consistently better than 99.9%.

INPUT/OUTPUT DIAGRAMS

Input



Output



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage
with Respect to Ground ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs
(except during programming)..... −0.5 to +V_{CC} Max.
DC Voltage Applied to
Outputs During Programming ..... 16 V
Output Current Into Outputs
During Programming
(Maximum duration of 1 second)..... 200 mA
DC Input Voltage..... −0.5 to +5.5 V
DC Input Current..... −30 to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A)..... 0 to +75°C
Supply Voltage (V_{CC}) .....+4.75 to +5.25 V

Extended Commercial (E) Devices
Temperature (T_A)..... −55°C Min.
Temperature (T_C)..... +125°C Max.
Supply Voltage (V_{CC}) .....+4.50 to +5.50 V

Military (M) Devices
Temperature (T_A)..... −55°C Min.
Temperature (T_C)..... +125°C Max.
Supply Voltage (V_{CC}) .....+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified; included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted

Parameter Symbol	Parameter Description	Test Conditions				Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	18P8A, 18P8B	COM'L	2.4	3.5		Volts
				18P8L, 18P8AL					
			I_{OH} = −2 mA	18P8Q					
			I_{OH} = −2 mA	(all versions)	MIL				
V_{OL}	Output LOW Voltage		I_{OL} = 24 mA	18P8A, 18P8B	COM'L			0.50	Volts
				18P8L, 18P8AL					
			I_{OL} = 12 mA	18P8Q					
			I_{OL} = 12 mA	A, B, AL, L	MIL				
			I_{OL} = 8 mA	18P8Q					
V_{IH} (Note 2)	Input HIGH level	Guaranteed Input Logical HIGH Voltage for All Inputs				2.0			Volts
V_{IL} (Note 2)	Input LOW level	Guaranteed Input Logical LOW Voltage for All Inputs						0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V					−20	−100	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V						25	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V						1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 3)				−30	−60	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max.		18P8A, 18P8B				180	mA
				18P8L, 18P8AL				90	
				18P8Q				55	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA					−0.9	−1.2	Volts
I_{OZH}	Output Leakage Current	V_{CC} = Max., V_{IL} = 0.8 V, V_{IH} = 2.0 V		V_O = 2.7 V				100	μA
I_{OZL}				V_O = 0.4 V				−250	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz					6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz					9		

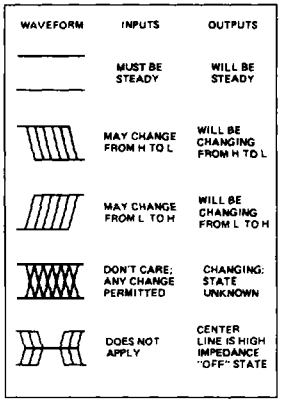
Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz	9	

Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

KEY TO SWITCHING WAVEFORMS



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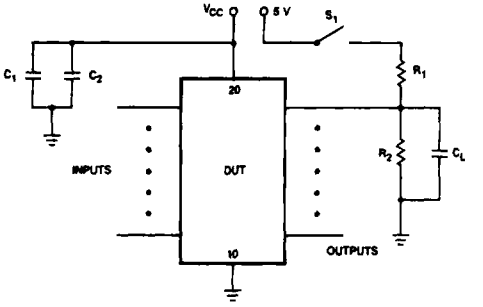
SWITCHING TEST CIRCUIT



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Note: C_1 and C_2 are to bypass V_{CC} to ground during testing.

TEST OUTPUT LOADS

Power Grade	R_1 (Ω)		R_2 (Ω)		C_L (pF)	C_1 (μF)	C_2 (μF)
	STD	APL	STD	APL	STD/APL	STD/APL	STD/APL
18P8B A AL L	200	390	390	750	50	0.1	0.01
18P8Q	390	600	750	1200	50	0.1	0.01

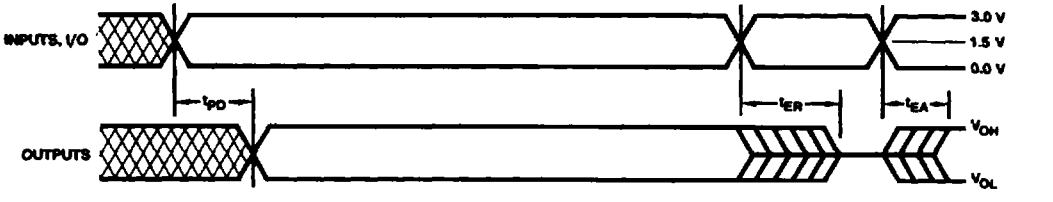
STD = AMD "Standard" products
APL = AMD "Approved Products List" products

SWITCHING CHARACTERISTICS over operating range unless otherwise specified; included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted

Parameter	Description	Commercial						Military						Units
		18P8B		18P8A/AL		18P8L/Q		18P8B		18P8A/AL		18P8L/Q		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
t_{PD}	Input to Output Delay	12	15	15	25	25	35	12	20	15	30	25	40	ns
t_{EA}	Input to Output Enable	12	15	15	25	25	35	12	20	15	30	25	40	ns
t_{ER}	Input to Output Disable	12	15	15	25	25	35	12	20	15	30	25	40	ns

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. t_{PD} is tested with switch S_1 closed and C_L = 50 pF.
3. For three-state output, output enable times are tested with C_L = 50 pF to the 1.5 V level; S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. Output disable times are tested with C_L = 5 pF. HIGH to high-impedance tests are made to an output voltage of V_{OH} – 0.5 V with S_1 open; LOW to high-impedance tests are made to the V_{OL} + 0.5 V level with S_1 closed.

SWITCHING WAVEFORM



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PROGRAMMING

Each AMD PAL fuse is programmed with a simple sequence of voltages applied to two control pins (1 and 11) and a programming voltage pulse applied to the output being programmed. Addressing of the 2600 element fuse array is accomplished with TTL and V_{HH} levels on eight input pins (five select the input line number and three select the product term number). V_{CC} is maintained at a normal level throughout the programming and verify cycle — no extra high V_{CC} levels are required.

The necessary sequence of levels for programming any fuse is shown in the Programming Waveforms. The address of each fuse in terms of Input Line Number and Product Term Line Number is defined by the Fuse Address Tables 1 and 2. Current, voltage and timing requirements for each pin are specified in the Programming Parameter Table on the following page.

After all programming has been completed, the entire array should be reverified at V_{CCL} and again at V_{CCH}. Reverification can be accomplished by reading all eight outputs in parallel rather than one at a time. The array fuse verification cycle checks that the correct array fuses have been blown and can be sensed by the outputs.

AMD PALs have been designed with many internal test features that are used to assure high programming yield and correct logical operation for a correctly programmed part.

An additional fuse is provided on each AMD PAL circuit to prevent unauthorized copying of AMD PAL fuse patterns when design security is desired. Blowing the security fuse blocks entry to the fuse pattern verify mode.

To blow the security fuse:

1. Power to V_{CCP}
2. Raise Pin 11 to V_{OP}
3. Pulse Pin 5 to V_{HH} for 50 microseconds 10 times
4. Reverify the entire array. A secured device will verify as if all fuses in the array are blown

Note that parts with the security fuse blown may not be returned as programming rejects.

AMD PALs normally have high programming yields (> 98%). Programming yield losses are frequently due to poor socket contact or equipment out of calibration or improperly used.

Design Aid Software for AmPAL18P8

Software Vendor	Software Package	Comments
P-CAD Systems (408) 971-1300	CUPL	
Advanced Micro Devices (408) 732-2400	AmCUPL	Developed and supported by P-CAD Systems
Data I/O (206) 881-6444	ABEL	

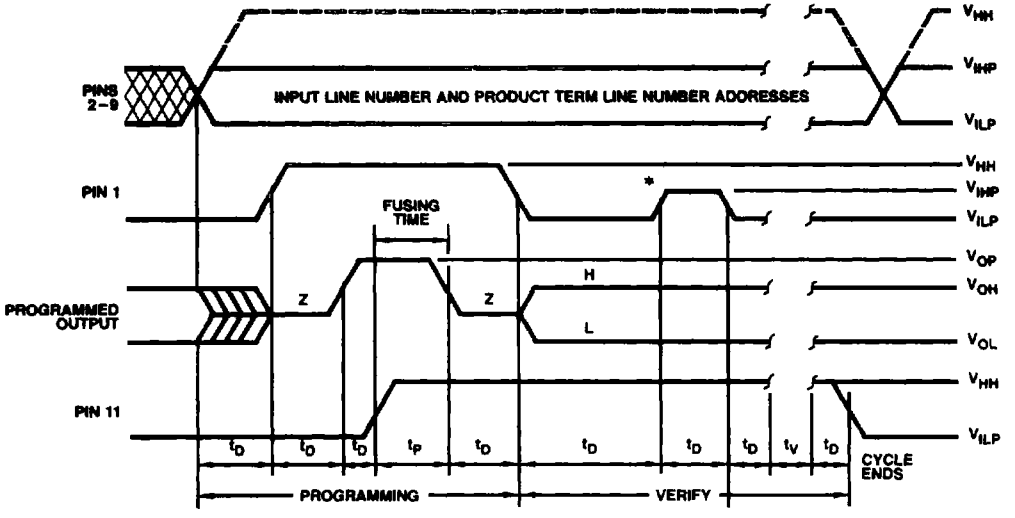
AMD Qualified Programmers

Name	Programmer Model(s)	AMD PAL Personality Module	Socket Adapter
Data I/O 10525 Willow Road N.E. Redmond, WA 98052	System 19, 29	950-1942-0044	303A-004, rev 3 or newer
	60	N/A	360A-001, rev 4 or newer
Stag Microsystems 528-5 Weddell Drive Sunnyvale, CA 94086	Model PPZ	Revision 19	On Board
	ZL30	On Board Module (rev 38 or newer)	
Structured Design 1700 Wyatt Drive Suite 3 Santa Clara, CA 95084	SD-1000J	Under Development	On Board
Valley Data Sciences 2426 Charleston Road Mountain View, CA 94043	160 Series	Under Development	On Board
Digelec 586 Weddell Drive Suite 1 Sunnyvale, CA 94089	803 Series	Under Development	Under Development
JMC 2999 Monterey Rd. Monterey, CA 93940	PROMAC P3	On-Board Module rev 2.0	On Board

PROGRAMMING PARAMETERS $T_A = 25°C$

Parameters	Description		Min.	Typ.	Max.	Units
V_{HH}	Control Pin Extra High Level	Pins 1 & 11 @ 10 – 40 mA	10	11	12	Volts
	Address Extra High Level	Pins 4, 5, and 9, @ V_{HH}				
V_{OP}	Program Voltage Pins 12 – 19 @ 15 – 200 mA		14	15	16	Volts
V_{IHP}	Input High Level During Programming and Verify		2.4	5	5.5	Volts
V_{ILP}	Input Low Level During Programming and Verify		0.0	0.3	0.5	Volts
V_{CCP}	V_{CC} During Programming @ I_{CC} = 50 – 200 mA		5	5.2	5.5	Volts
V_{CCL}	V_{CC} During First Pass Verification @ I_{CC} = 50 – 200 mA		4.4	4.5	4.6	Volts
V_{CCH}	V_{CC} During Second Pass Verification @ I_{CC} = 50 – 200 mA		5.4	5.5	5.6	Volts
V_{Blown}	Successful Blown Fuse Source Level @ Output			0.3	0.5	Volts
dV_{OP}/dt	Rate of Output Voltage Change		20		250	V/μsec
dV_{11}/dt	Rate of Fusing Enable Voltage Change (pin 11 rising edge)		20		1000	V/μsec
t_P	Fusing Time First Attempt		10	50	100	μsec
	Subsequent Attempts (maximum of 8)		4	5	10	msec
t_D	Delays Between Various Level Changes		100	1000	15000	ns
t_V	Period During which Output is Sensed for V_{Blown} Level		100	1000	15000	ns
V_{ONP}	Pull-Up Voltage On Outputs Not Being Programmed		V_{CCP} – 0.3	V_{CCP}	V_{CCP} + 0.3	Volts
R	Pull-Up Resistor On Outputs Not Being Programmed		1.9	2	2.1	kΩ

PROGRAMMING WAVEFORMS



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*The Pulse to V_{IHP} on pin 1 is unnecessary for fuse verification on combinatorial parts. It is used as a clock pulse on registered parts and is kept to maintain algorithm compatibility.

TABLE 1. INPUT ADDRESSING

Input Line Number	Input Line Number Address Pin States				
	9	8	7	6	5
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H
32	HH	L	L	L	L
33	HH	L	L	L	H
34	HH	L	L	H	L
35	HH	L	L	H	H
36*	HH	L	H	L	L

L = V_{ILP}
H = V_{IHP}
HH = V_{HH}
*Output polarity.

SIMPLIFIED PROGRAMMING DIAGRAM

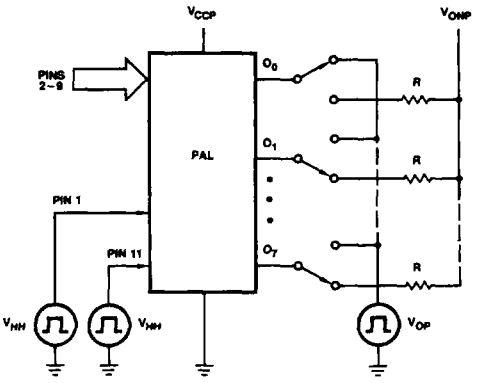

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TABLE 2. PRODUCT TERM ADDRESSING

Product Term Line Number								Product Term Select Address Pin		
								4	3	2
0	9	18	27	36	45	54	63	L	L	L
1	10	19	28	37	46	55	64	L	L	H
2	11	20	29	38	47	56	65	L	H	L
3	12	21	30	39	48	57	66	L	H	H
4	13	22	31	40	49	58	67	H	L	L
5	14	23	32	41	50	59	68	H	L	H
6	15	24	33	42	51	61	69	H	H	L
7	16	26	34	43	52	61	70	H	H	H
8	17	26	35	44	53	62	71	HH	L	L
P	P	P	P	P	P	P	P	HH	L	H
Pin 19	Pin 18	Pin 17	Pin 16	Pin 15	Pin 14	Pin 13	Pin 12	L = V_{ILP} H = V_{IHP} HH = V_{HH}		
Programming Access and Verify Pin										

Output Enable Logical P.T.s

Output Polarity